REMARKS

Claims 1 - 20 were pending in the application. Claims 1-20 have been cancelled. Claims 21-37 have been added. Claims 21-37 accordingly remain pending in the application.

Applicant notes that added claims 21-37 are similar to previously pending claims 1-17.

35 U.S.C. §112 Rejection

Claims 10-20 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Applicant has cancelled Claims 17-20; therefore, the rejection of these claims is believed moot. Added claims 30 and 32, which are similar to previously pending claims 10 and 12, respectively, have been written to overcome this rejection.

35 U.S.C. §102 Rejections

Claims 1-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Klug et al. (U.S. Patent # 5,226,152). Applicant respectfully traverses this rejection.

Added Claims 21-37 are believed to patentably distinguish over Klug.

Klug teaches N redundant processors operating in functional lockstep synchronization for maintaining system integrity. Specifically, Klug teaches "For each write operation which is to be compared, each processor 1 through N writes the output into an appropriate register 10, 20, etc." (Klug, Column 3, Lines 26-28, Figure 2) Also, Klug teaches "When all of the N processors have written into their appropriate registers, compare logic 15 checks the contents of each of the processor's registers. If the contents of the registers match, the signal on the corresponding wait lead is negated or removed and the processors are allowed to continue processing." (Klug, Column 3, Lines 42-48, Figure 2)

On the other hand, Applicant respectfully submits that Klug fails to teach or suggest "each of said processors has a processor identification register which is read/writeable and is operable to store in said register data representative of a processor identification, said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register" as recited in claim 21. In accordance, claim 21 is believed to patentably distinguish over Klug.

Claims 22-29 depend on claim 21 and are therefore believed to patentably distinguish over Klug for at least the reasons given above.

In addition, Applicant further respectfully submits that Klug fails to teach or suggest "a processor identification register coupled to said interface, said register is read/writeable and is configured to store data representative of a processor identification, wherein said processor is responsive to a masking condition, to write a common predefined data value received via said I/O bus into said processor identification register, wherein said predefined data value is common to said processing sets and is operable to mask said processor identification" as recited in claim 30. In accordance, claim 30 is believed to patentably distinguish over Klug.

Claim 31 depends on claim 30 and is therefore believed to patentably distinguish over Klug for at least the reasons given above.

Claim 32 recited features similar to those highlighted above with regard to claim 21 and is therefore believed to patentably distinguish over Klug for at least the reasons given above in the paragraphs discussing claim 21. Claims 33-35 depend on claim 32 and are therefore believed to patentably distinguish over Klug for the same reasons.

Claim 36 recited features similar to those highlighted above with regard to claim 30 and is therefore believed to patentably distinguish over Klug for at least the reasons given above in the paragraphs discussing claim 30. Claim 37 depends on claim 36 and is therefore believed to

patentably distinguish over Klug for the same reasons.

Claims 1-20 were also rejected under 35 U.S.C. §102(b) as being anticipated by Kobasyashi et al. (GB 2,290,891). Applicant respectfully traverses this rejection.

Added Claims 21-37 are believed to patentably distinguish over Kobasyashi.

Kobasyashi teaches a method for initializing a multiprocessor system while resetting defective CPU's detected during operation. Specifically, Kobasyashi teaches "an identifier setting register, connected to the common bus, capable of assigning to and reading from an arbitrary CPU a CPU number, for designating assigned CPU numbers to the respective CPUs." (Kobasyashi, Page 8, Lines 9-12) Also, Kobasyashi teaches "the identifier setting register designates the CPU numbers in the predetermined order only to normal CPUs; the reset controller cuts off defective CPUs from the common bus." (Kobasyashi, Page 9, Lines 11-13)

On the other hand, Applicant respectfully submits that Kobasyashi fails to teach or suggest "said processors being arranged, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said processor identification register" as recited in claim 21. In accordance, claim 21 is believed to patentably distinguish over Kobasyashi.

Claims 22-29 depend on claim 21 and are therefore believed to patentably distinguish over Kobasyashi for at least the reasons given above.

In addition, Applicant further respectfully submits that Kobasyashi fails to teach or suggest "said processor is responsive to a masking condition, to write a common predefined data value received via said I/O bus into said processor identification register, wherein said predefined data value is common to said processing sets and is operable to mask said processor identification" as recited in claim 30. In accordance, claim 30 is believed to patentably distinguish over Kobasyashi.

Claim 31 depends on claim 30 and is therefore believed to patentably distinguish over Kobasyashi for at least the reasons given above.

Claim 32 recited features similar to those highlighted above with regard to claim 21 and is therefore believed to patentably distinguish over Kobasyashi for at least the reasons given above in the paragraphs discussing claim 21. Claims 33-35 depend on claim 32 and are therefore believed to patentably distinguish over Kobasyashi for the same reasons.

Claim 36 recited features similar to those highlighted above with regard to claims 30 and is therefore believed to patentably distinguish over Kobasyashi for at least the reasons given above in the paragraphs discussing claim 30. Claim 37 depends on claim 36 and is therefore believed to patentably distinguish over Kobasyashi for the same reasons.

In light of the foregoing amendments and remarks, Applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If a phone interview would speed allowance of any pending claims, such is requested at the Examiner's convenience.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-80100/BNK.

Respectfully submitted,

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